PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Williams, Anthony David	)	**Examiner:** Nguyen, Linh M.
		)	
Serial No.:	10/713,717	)	**Art Unit:** 2816
		)	
Filing Date:	November 14, 2003	)	**Atty. Docket No.** 030772

Title: FREQUENCY SYNTHESIZER HAVING PLL WITH AN ANALOG PHASE DETECTOR

DECLARATION OF MR. A. DAVID WILLIAMS UNDER 37 C.F.R. 1.131

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir :

I, A. David Williams, declare as follows:

1. I am the sole named inventor for the above-captioned patent application (hereinafter "the subject application").

2. I am a citizen of the United Kingdom and I reside in Aptos, California 95003.

3. I am over the age of eighteen and am competent to makes the statements in this Declaration.

4. I am currently employed by Teledyne Technologies Incorporated, the assignee of the subject application.

5. I conceived of the subject matter described and claimed in the subject application, including the subject matter of amended claim 19, prior to April 1, 2003.

6. In support of the conception date alleged above, I enclose a page from my engineering notebook. This document discloses a frequency synthesizer with a phase lock loop (PLL) that includes an auxiliary digital frequency detector that causes a "steering current" to flow into or out of the loop filter of the PLL. This in turn causes the voltage applied to the VCO by the loop filter to ramp up or down at a rate set by a time constant of the loop filter. When the VCO reaches a frequency such that the output signal from the analog phase mixer detector is within the bandpass range of the loop filter, phase lock for the PLL is achieved. The depicted frequency synthesizer performs the method of amended claim 19.

7. The date from the attached engineering notebook page has been redacted. The redacted date is prior to April 1, 2003.

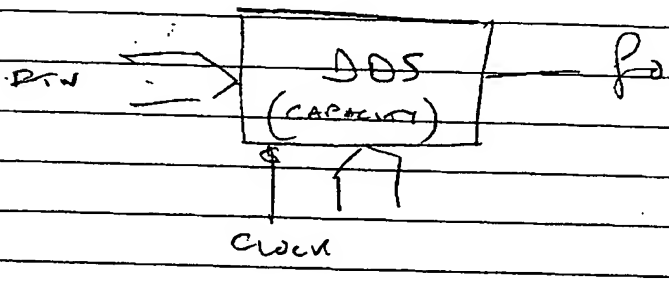
8. I reduced the invention to practice not long after I conceived of the invention. I believe that I acted with continuous due diligence to reduce the invention to practice from a date prior to April 1, 2003 until eventual reduction to practice.

9. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or document or any registration resulting therefrom.

Date 10/12/2005

A. David Williams

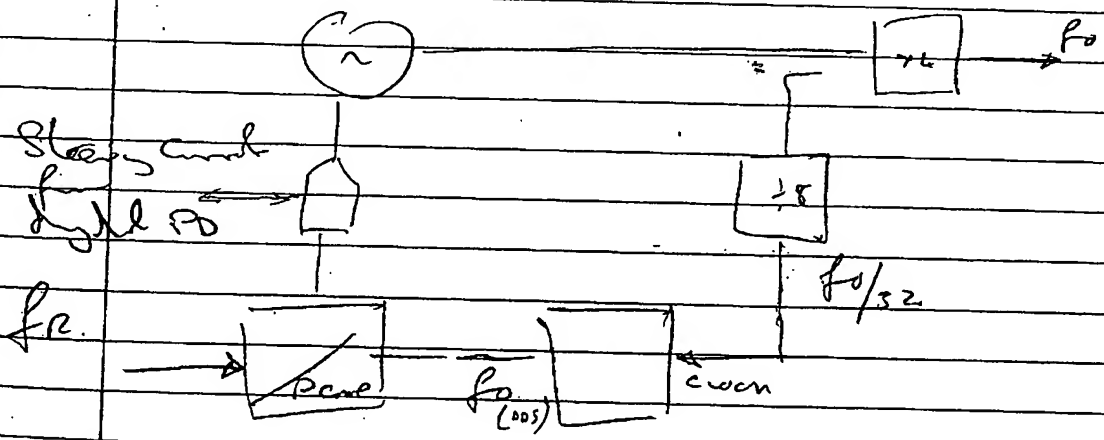
DDS IDL SYNTH



$$f_o = \frac{(FTW) \times f_c}{2^{(CAP)}}$$

FOR 32 BIT ACCUMULATOR.

$$f_o = \frac{(FTW) \times f_c}{2^{32}}$$



IN DDS "IN THE LOOP"

$$f_R = \frac{(FTW) \times f_o/32}{2^{32}}$$

$$f_R = \frac{(FTW) \times f_o}{2^{32} \times 32} = \frac{(FTW) \times f_o}{2^{37}}$$